

In the Specification:

Page 10, last paragraph amended as:

A1
The bottom and top of channel 204 may be defective. Particularly if the epitaxial layer is thin, the region is likely to be extremely small and may not be significant to the formation of the device. However, if it is necessary to remove these regions, two processes are available to do so at small but tolerable, degrade of device width control. Specifically, a spacer could be deposited similar to that of spacer 302 of Figure 3B, but etched lower to uncover the top of the epitaxial region. After this spacer is formed, the buried oxide is etched underneath the spacer as shown on the left side of Figure 12. Alternatively, a thin composite spacer may be used. In this case, the bottom of the spacer are isotropically etched to uncover the top and bottom regions. The height of the spacer (overetch) is determined by the undercut necessary to reach the epitaxial region at the bottom of the spacer, as shown on the right side of Figure 12. After the defective regions are etched, the spacers are removed selectively to the epitaxial regions and the buried oxide layer before proceeding to following processing steps. It should be noted that it is also possible to perform the procedure described above after the spacer shown in Figure 4B is removed with the spacers of the above described procedure being removed before further processing.

In the Claims:

- A2
A3 C5
1. (Amended) A method of forming a field effect transistor (FET) transistor, comprising:
providing a substrate;
forming a layer on the substrate, the layer having a side surface;
forming an epitaxial channel on the side surface, the channel having a first sidewall;
removing the layer for exposing a second sidewall of the channel;
forming a gate adjacent to at least one of the sidewalls of the channel.
 15. (Amended) The method as recited in claim 14, wherein the forming step comprises the steps of:

BUR919990300US1
SN 09/691,353